FILE 'INPADOC, WPIX, JAPIO, HCAPLUS' ENTERED AT 16:55:59 ON 12 MAR 2002

E TW01-90102493/PRN,AP
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L1 21 S HANNSTAR?/PA,CS

L2 15 S ("SHIH PO SHENG"/AU OR "SHIH PO SHENG"/IN)

L3 36 S (L1 OR L2)

L4 105681 S (ULTRA OR ULTRATHIN)

L5 0 S L3 AND L4

L6 1777 S (ULTRA THIN OR ULTRATHIN)(2A)(TFT OR TRANSISTOR OR CHANNEL OR POLYSI OR POLYSILICON OR (SI OR SILICON))

L7 15 S L6 AND (TFT OR THIN FILM TRANSISTOR OR THINFILM TRANSISTOR) AND (POLYSI OR POLYSILICON OR (POLY OR POLYCRYST?)(2A)(SI OR SILICON))

L8 4 S JP 05063195/PN

L9 816 S (30 OR 25 OR 20 OR 15 OR 19)(W)(ANGSTROM OR NM OR NANOMETER OR AA)(4A)(TFT OR TRANSISTOR OR CHANNEL OR POLYSI OR POLYSILICON OR (SI OR SILICON))

L10 14 S L9 AND (TFT OR THIN FILM TRANSISTOR OR THINFILM TRANSISTOR) AND (POLYSI OR POLYSILICON OR (POLY OR POLYCRYST?)(2A)(SI OR SILICON))

L11 10 S L10 NOT (L7 OR L8)

L7 ANSWER 5 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:872566 HCAPLUS
DN 136:159392
TI A novel self-aligned double-gate **TFT** technology
AU Zhang, Shengdong; Han, Ruqi; Sin, Johnny K. O.; Chan, Mansun
CS The Institute of Microelectronics, Peking University, Beijing, Peop. Rep. China
SO IEEE Electron Device Letters (2001), 22(11), 530-532 Nov. 2001
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB In this letter, a novel self-aligned double-gate (SADG) **thin-film transistor** (**TFT**) technol. is proposed and exptl. demonstrated for the first time. The self-alignment between the top-gate and bottom-gate (BG) is realized by a noncrit. chem.-mech. polishing (CMP) step. An **ultrathin channel** and a thick source/drain, that allow better device performance and lower source/drain resistance, are also automatically achieved. N-channel **poly-Si TFTs** are fabricated with max. processing temp. below 600.degree.. Metal-induced unilateral crystn. (MIUC) is used for **poly-Si** grain size enhancement. The fabricated SADG **TFT** exhibits sym. bidirectional transfer characteristics when the polarity of source/drain bias is interchanged. The on-current under double-gate operation is more than two times the sum of that under TG and BG operation.
ST self aligned **TFT** double gate
IT **Thin film transistors**
(self-aligned double-gate **TFT** technol.)
IT **Thin film transistors**
(self-aligned double-gate **TFT** technol.)

L7 ANSWER 10 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:496628 HCAPLUS
DN 133:158264
TI A novel **ultra-thin channel poly-Si TFT** technology
AU Zhang, Sheng-dong; Han, Ru-qi; Guan, Xu-dong; Liu, Xiao-yan; Wang, Yang-yuan
CS Institute of Microelectronics, Peking University, Beijing, 100871, Peop. Rep. China
SO Bandaoti Xuebao (2000), 21(4), 317-324
CODEN: PTTPDZ; ISSN: 0253-4177
PB Kexue Chubanshe
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB A novel low temp. **poly-Si** (LTPS) **ultra-thin channel thin film transistor** (UTC-**TFT**) technol. is proposed. The UTC-**TFT** has an **ultra-thin channel** region (30 nm) and a thick drain/source region (300 nm). The **ultra-thin channel** region that can result in a lower grain-boundary trap d. in the channel is connected to the heavily-doped thick drain/source region through a lightly-doped overlapped region. The overlapped lightly-doped region provides an effective way for the elec. field to spread in the channel near the drain at high drain biases, thereby reducing the elec. field there significantly. Simulation results show the UTC-**TFT** experiences a 50% redn. in peak lateral elec. field compared to that of the conventional **TFT**. With the low grain-boundary trap d. and low drain elec. field, excellent current satn. characteristics and high drain breakdown voltage are achieved in the UTC-**TFT**. Moreover, this technol. provides the complementary LTPS-**TFTs** with more than 2 times increase in on-current, 3.5 times redn. in off-current compared to the conventional thick channel LTPS **TFTs**.
ST **polycryst silicon thin film transistor**
IT **Thin film transistors**

L7 ANSWER 1 OF 15 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1993-375498 [47] WPIX
DNC C1993-166962
TI **Thin film transistor** mfr. - by depositing electroconductive and insulating layers on silicon substrate, forming contact window, depositing **poly-silicon** and coating with photoresist, etc..
DC L03 U11
IN JEONG, S
PA (SMSU) SAMSUNG ELECTRONICS CO
CYC 1
PI KR 9303272 B 19930424 (199347)* H01L021-312
ADT KR 9303272 B KR 1990-16241 19901013
PRAI KR 1990-16241 19901013
IC ICM H01L021-312
AB KR 9303272 B UPAB: 19940111
Transistor is mfd. by (a) depositing an electroconductive layer and an insulating layer on an Si substrate by the CMOS process, forming a contact window and depositing a **polysilicon** layer or an amorphous Si layer by CVD; (b) coating a photoresist on the layer, exposing a channel region by photoetching to form an **ultra-thin** **polysilicon** layer of the channel region and depositing a gate oxide film (6) by CVD or heat oxidisation; and (c) forming a contact window on the film, depositing a **polysilicon** layer, implanting an impurity and then coating a photoresist and patterning it to form a self alignment source and drain.
FS CPI EPI

L8 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:550508 HCAPLUS
DN 119:150508
TI Manufacture of thin-film transistors
IN Hirota, Masanori; Fuse, Mario; Asai, Ichiro
PA Fuji Xerox Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L029-784
ICS H01L027-12
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05063195	A2	19930312	JP 1991-40147	19910306 <--

AB This manuf. includes (a) forming a base insulator film on an insulator substrate; (b) forming holes in the locations of the insulator film, which correspond to source and drain electrodes; (c) forming a poly-Si film, and doping it with an impurity (e.g., P); (d) removing the poly-Si excluding that filling the holes; (e) forming an ultra-thin active layer; (f) forming source and drain electrodes in part of the active layer; (g) depositing a gate-insulator film; (h) forming a gate electrode; (i) forming an interlayer insulator film; (j) forming contact holes in the insulator film, which reach the source and drain electrodes; and (h) forming interconnection electrodes connected with the source and drain electrodes across the contact holes. The thin-film has small contact resistance.

ST thin film transistor small contact resistance
IT Transistors
(field-effect insulated-gate, with small resistance, manuf. of)
IT 11099-22-2P
RL: IMF (Industrial manufacture); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(interconnection electrodes, thin-film transistor contg., manuf. of)
IT 7440-21-3P, Silicon, uses
RL: IMF (Industrial manufacture); PRP (Properties); PREP (Preparation)
(polycryst., doped, thin-film transistors contg., manuf. of)
IT 7440-21-3P, Silicon, uses
RL: IMF (Industrial manufacture); PRP (Properties); PREP (Preparation)
(polycryst., doped, thin-film transistors contg., manuf. of)

L7 ANSWER 3 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1991-020046 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN KOBAYASHI KAZUNORI; NAKAMURA AKIRA; YAMAMOTO ATSUYA; FUJII EIJI; SENDA KOJI
PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
PI JP 03020046 A 19910129 Heisei
AI JP1989-155395 (JP01155395 Heisei) 19890616
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1054, Vol. 15, No. 143, P. 62 (19910411)
IC ICM (5) H01L021-336
ICS (5) H01L029-784
AB PURPOSE: To reduce a contact resistance of a source.cntdot.drain by incorporating a step of slightly retaining a gate oxide film on the source.cntdot.drain of a **thin film transistor**
.
CONSTITUTION: An oxide film 13 formed on a **polysilicon** layer 12 is retained in an etching step of an oxide film except at a position directly under a gate electrode 14. That is, since energy of certain degree is lost due to the film 13 on the **polysilicon** 12, the energy of an impurity to be implanted is reduced when it arrives at the **polysilicon** 12. Therefore, even in case of an **ultrathin** film **polysilicon**, the implanted impurity is punched through the **polysilicon** thin film, but not arrived at a quartz substrate 11 but collected into the **polysilicon** thin film, and the impurity concentration in the **polysilicon** is enhanced. Thus, the contact resistance of a source.cntdot.drain is reduced.

L7 ANSWER 6 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:867071 HCAPLUS
DN 136:94058
TI Comparison study of metal induced lateral crystallized and solid-phase crystallized **polycrystalline silicon thin film transistors** with different channel thickness
AU Jin, Zhonghe
CS Dept. of Information and Electronic Engineering, Zhejiang University, Hangzhou, 310027, Peop. Rep. China
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2001), 40(11), 6325-6326
CODEN: JAPNDE
PB Japan Society of Applied Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB N- and P-type **polycryst. silicon thin film transistors** are fabricated with channel thickness of 30 nm and 100 nm by metal induced lateral crystn. and conventional solid-phase crystn. of amorphous silicon. Significant improvement is obtained for the metal induced lateral crystn. devices by **ultrathin channel** layer. However, for solid-phase crystn. devices, improvement is not as significant. The possible reasons are proposed and discussed.
ST **silicon polycryst thin film transistor** channel thickness
IT **Thin film transistors**
(comparison study of metal induced lateral crystd. and solid-phase crystd. **polycryst. silicon thin film transistors** with different channel thickness)
IT **Thin film transistors**
(comparison study of metal induced lateral crystd. and solid-phase crystd. **polycryst. silicon thin film transistors** with different channel thickness)

L7 ANSWER 11 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:212713 HCAPLUS
DN 132:316432
TI **Ultrathin** elevated **channel poly-Si** **TFT** technology for fully integrated AMLCD system on glass
AU Zhang, Shengdong; Zhu, Chunxiang; Sin, Johnny K. O.; Li, J. N.; Mok, Philip K. T.
CS Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, Peop. Rep. China
SO IEEE Trans. Electron Devices (2000), 47(3), 569-575
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 74
AB A novel low-temp. **poly-Si** (LTPS) **TFT** technol. called the **ultrathin** elevated **channel** **TFT** (UT-ECTFT) technol. is proposed. Devices fabricated using this technol. have an **ultrathin channel** region (300 .ANG.) and a thick drain/source region (3000 .ANG.). The **ultrathin channel** region is connected to the heavily doped thick drain/source region through a lightly doped overlapped region. The **ultrathin channel** region is used to obtain a low grain-boundary trap d. in the channel, and the overlapped lightly doped region provides an effective way for elec. field spreading at the drain thereby reducing the elec. field there significantly. With the low grain-boundary trap d. and low drain elec. field, excellent current satn. characteristics and high drain breakdown voltage are obtained in the UT-ECTFT. Moreover, this technol. provides complementary LTPS **TFT** 's with more than two times increase in on-current, 3.5 times redn. in off-current compared to conventional thick-channel LTPS **TFT**'s.
ST **ultrathin** elevated **channel polysilicon** **TFT** technol; liq crystal display **TFT** transistor technol
IT Liquid crystal displays
(active-matrix; **ultrathin** elevated **channel** **poly-Si TFT** technol. for fully integrated AMLCD system on glass)
IT **Thin film transistors**

L7 ANSWER 12 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:741249 HCAPLUS
DN 131:330710
TI A novel **ultrathin** elevated **channel** low-temperature **poly-Si TFT**
AU Zhang, Shengdong; Zhu, Chunxiang; Sin, Johnny K. O.; Mok, Philip K. T.
CS Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, Hong Kong
SO IEEE Electron Device Lett. (1999), 20(11), 569-571
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB A novel **ultrathin** elevated **channel thin-film transistor** (UT-ECTFT) made using low-temp. **polycryst. silicon** (**poly-Si**) is proposed. The structure has an **ultrathin channel** region (300 .ANG.) and a thick drain/source region. The thin channel is connected to the heavily doped drain/source through a lightly doped overlapped region. The lightly doped overlapped region provides an effective way to spread out the elec. field at the drain, thereby reducing significantly the lateral elec. field there at high drain bias. Thus, the UT-ECTFT exhibits excellent current satn. characteristics even at high bias (Vds = 30 V, Vgs = 20 V). Moreover, the UT-ECTFT has more than two times increase in on-state current and 3.5 times redn. in off-state current compared to conventional thick channel **TFT**'s.
ST **silicon polycryst** elevated channel **thin film transistor**

L7 ANSWER 13 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:291323 HCAPLUS
DN 131:26342
TI Performance of **thin-film transistors** with **ultrathin** Ni-MILC **polycrystalline silicon** channel layers
AU Jin, Zhonghe; Kwok, Hoi S.; Man, Wong
CS Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, Peop. Rep. China
SO IEEE Electron Device Lett. (1999), 20(4), 167-169
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB High-performance, low-temp. processed **thin-film transistors** (**TFT**'s) with **ultrathin** (30-nm) metal induced laterally crystd. (MILC) channel layers were fabricated and characterized. Compared with the MILC **TFT**'s with thicker (100 nm) channel layers, the ones with the 30-nm channel layers exhibit lower threshold voltage, steeper subthreshold slope, and higher transconductance.
ST **polysilicon** channel **thin film transistor** nickel induced laterally crystd

L7 ANSWER 15 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:118218 HCAPLUS
DN 116:118218
TI Low temperature **polysilicon TFTs** using solid phase crystallization of very thin films and an electron cyclotron resonance chemical vapor deposition gate insulator
AU Little, Thomas W.; Takahara, Kenichi; Koike, Hideki; Nakazawa, Takashi; Yudasaka, Ichio; Ohshima, Hiroyuki
CS TFT Res. Lab., Seiko Epson Corp., Suwa, 392, Japan
SO Jpn. J. Appl. Phys., Part 1 (1991), 30(12B), 3724-8
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
AB Low temp. (T .ltoreq.600.degree.) **polycryst. Si thin film transistors** (**poly-Si TFTs**) were fabricated by solid phase crystn. (SPC) of amorphous Si films deposited by low pressure CVD. These **TFTs** are distinguished by the very thin nature of the channel Si layer (25 nm) and the use of an SiO2 gate insulator deposited by electron cyclotron resonance CVD. The present process eliminates the need for hydrogenation and produces mobilities greater than 20 cm2/V.s and on/off current ratios greater than 107.
ST transistor **polysilicon** film crystn amorphous silicon; solid crystn silicon **polysilicon** film transistor; silica gate CVD **polysilicon** film transistor
IT Crystallization
(solid-phase, of **ultrathin** amorphous **silicon**, for **polysilicon** film transistor)

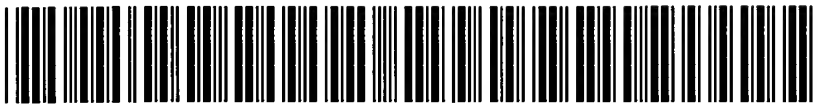
L11 ANSWER 2 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-478405 [42] WPIX
DNN N2000-356557 DNC C2000-144326
TI Polycrystalline **thin film transistor** for liquid crystal display device, has source and drain formed on channel of **polycrystalline silicon** film with preset thickness.
DC L03 P81 U11 U12 U14
PA (HITA) HITACHI LTD
CYC 1
PI JP 2000174278 A 20000623 (200042)* 5p H01L029-786
ADT JP 2000174278 A JP 1998-341348 19981201
PRAI JP 1998-341348 19981201
IC ICM H01L029-786
ICS G02F001-136; H01L021-336
AB JP2000174278 A UPAB: 20000905
NOVELTY - A source (3) and drain (4) having identical dopant concentration are formed on a channel (1) comprising a **polycrystalline silicon** film (2). The thickness of **polycrystalline silicon** film is **30 nm** or less.
DETAILED DESCRIPTION - The transistor has channel (1) deposited on a glass substrate via a buffer layer. A gate insulating film and a gate electrode are sequentially deposited on the channel. An INDEPENDENT CLAIM is also included for **thin film transistor** manufacturing method.
USE - For liquid crystal display device.
ADVANTAGE - The **thin film transistor** of high driving force is obtained.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of **thin film transistor**.
Channel 1
Polycrystalline silicon film 2
Source 3
Drain 4
Dwg.1/5
FS CPI EPI GMPI
FA AB; GI
MC CPI: L03-G05A; L04-C10B; L04-E01
EPI: U11-C18A3; U12-B03A; U14-K01A2
DRN 1666-S

L11 ANSWER 8 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:567226 HCAPLUS
DN 125:210379
TI Polycrystal formation by excimer laser annealing and **thin-film transistors**
IN Maekawa, Shigeki; Furuta, Mamoru; Tsutsu, Hiroshi
PA Matsushita Electric Ind Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-20
ICS C30B030-00; H01L021-268; H01L027-12; H01L029-786; H01L021-336
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 73, 75
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08181069	A2	19960712	JP 1994-325177	19941227
	CN 1131340	A	19960918	CN 1995-119449	19951227
	CN 1050221	B	20000308		
	US 5766989	A	19980616	US 1995-579140	19951227
PRAI	JP 1994-325177	A	19941227		
	JP 1995-3631	A	19950113		

AB The title formation of **polycrystal Si** thin-film involves 1st excimer laser annealing an amorphous Si thin-film on a substrate to give a microcryst. (av. crystal diam. .ltoreq.**20 nm**) **Si** thin-film followed by 2nd excimer laser annealing the microcryst. Si thin-film to give a **polycryst. Si** thin-film. The **polycryst. Si** thin-film is provided for fabrication of **thin-film transistors**. The 2-staged annealing process gives the Si films evenly distributed crystn. over the substrate.
ST silicon microcryst excimer laser annealing transistor
IT Lasers
(excimer, polycrystal formation by excimer laser annealing and **thin-film transistors**)
IT Transistors
(field-effect insulated-gate, polycrystal formation by excimer laser annealing and **thin-film transistors**)
IT Annealing
(laser-induced, polycrystal formation by excimer laser annealing and **thin-film transistors**)
IT Crystallization
(micro-, polycrystal formation by excimer laser annealing and **thin-film transistors**)
IT Crystallization
(micro-, polycrystal formation by excimer laser annealing and **thin-film transistors**)

US 0993084705P1



Creation date: 11-05-2003
Indexing Officer: TLO - TRUC P LO
Team: OIPEBackFileIndexing
Dossier: 09930847

Legal Date: 03-13-2002

No.	Doccode	Number of pages
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Total number of pages: 30

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